AMENDMENTS TO THE CLAIMS

1. (currently amended) A multibank DRAM macro allowing concurrent operations to independent banks, said macro comprising:
   (a) a plurality of DRAM memory banks, each bank respectively comprising:
      (i) an array of DRAM memory cells,
      (ii) bitlines and wordlines, respectively defining columns and rows of the array,
      (iii) a dedicated row address decoder circuit,
      ~~(iv) a column address decoder circuit,~~
      (iv) ~~(v)~~ dedicated spare rows and columns for redundancy,
   (b) at least one column address decoder circuit shared by at least two of said banks,
   (c~~b~~) a dedicated bank select input pin for each respective bank, each bank select input pin being brought out as a control pin at an interface to said macro, each bank select input pin controlling operation of its respective bank and allowing concurrent operations to independent banks, and
   (d~~e~~) a data path receiver / driver shared by at least two banks.

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2. (original) The DRAM macro of claim 1 further comprising (d) a master select input.

3. (currently amended) The DRAM macro of claim 2 wherein said bank select inputs pins are latched to a falling edge of a signal from said master select input.

4. (original) The DRAM macro of claim 1 wherein said macro further comprises a write enable input.

5. (original) The DRAM macro of claim 1 wherein said macro further comprises a page mode select input.

6. (currently amended) The DRAM macro of claim 1 wherein each bank further comprises (vi) at least one sense amplifier.

7. (original) The DRAM macro of claim 1 wherein each bank has capacity for about 1 Mb of data.

8. (original) The DRAM macro of claim 7 wherein said macro comprises at least 4 of said banks.

9. (currently amended) An integrated circuit device comprising a logic core and a DRAM macro wherein said DRAM macro is a multibank DRAM macro allowing concurrent operations to independent banks, said DRAM macro comprising:

(a) a plurality of DRAM memory banks, each bank respectively comprising:

(i) an array of DRAM memory cells,

(ii) bitlines and wordlines, respectively defining columns and rows of the array,

(iii) a dedicated row address decoder circuit,

~~(iv) a column address decoder circuit ;~~

(iv) dedicated spare rows and columns for redundancy,

(b) at least one column address decoder circuit shared by at least two of said banks,

(c~~b~~) a dedicated bank select input pin for each respective bank, each

bank select input pin being brought out as a control pin at an interface to said macro, each bank select input pin controlling operation of its respective bank and allowing concurrent operations to independent banks, and

(de) a data path receiver / driver shared by at least two banks.

10. (currently amended) The integrated circuit device of claim 9 wherein said DRAM macro further comprises (ed) a master select input.

11. (currently amended) The integrated circuit device of claim 10 wherein said bank select inputs pins are latched to a falling edge of a signal from said master select input.

12. (original) The integrated circuit device of claim 9 wherein said DRAM macro further comprises a write enable input.

13. (original) The integrated circuit device of claim 9 wherein said DRAM macro further comprises a page mode select input.

14. (currently amended) The integrated circuit device of claim 9 wherein each bank of said DRAM macro further comprises (vi) at least one sense amplifier.

15. (original) The integrated circuit device of claim 9 wherein each bank of said DRAM macro has capacity for about 1 Mb of data.

16. (original) The integrated circuit device of claim 15 wherein said DRAM macro comprises at least 4 of said banks.

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